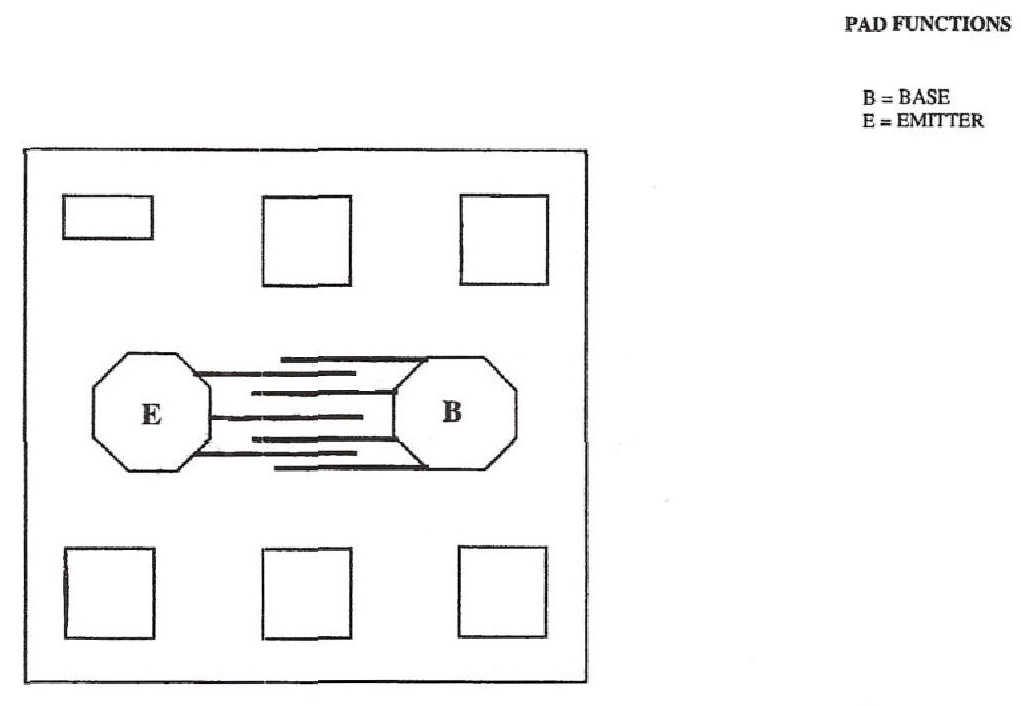
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.015”**



**.015”**

**Top Material: Au**

**Backside Material: Au**

**Bond Pad Size:**

**Backside Potential: Collector**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .015” X .015” DATE: 4/18/19**

**MFG: DIE TECH THICKNESS .0065” P/N: BFT93W**

**DG 10.1.2**

#### Rev B, 7/19/02